Power Monitor IC with Digital I²C Interface

FEATURES

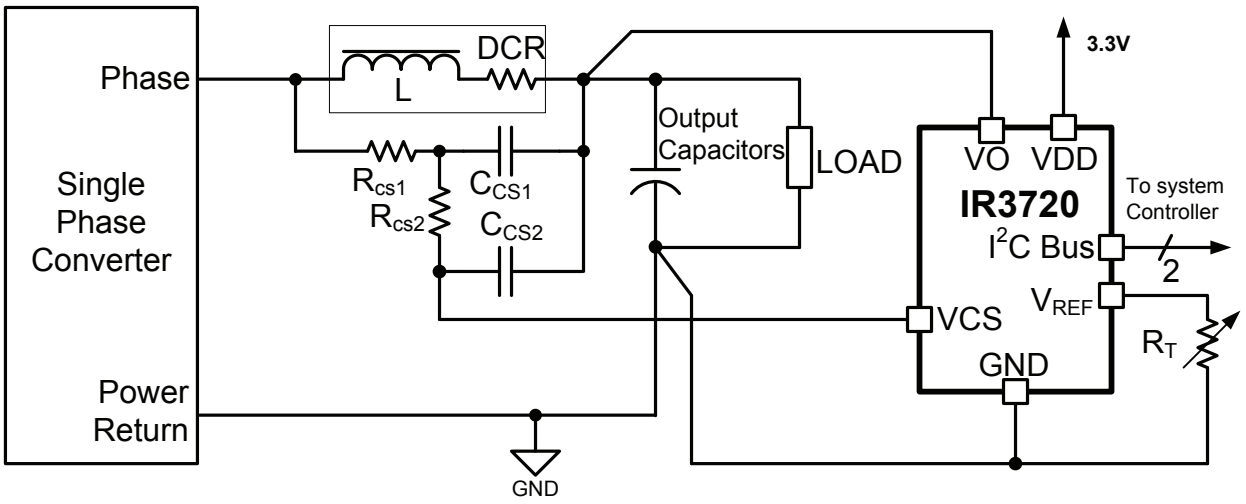
- Accurate *TruePower*™ monitor
  - Minimizes dynamic errors
  - Reports voltage, current, or power
- Digital interface
  - SMBus and I²C compatible
- Programmable averaging interval
- Flexible current sensing
  - Resistive or Inductor DCR
- Applications
  - Synchronous rectified buck converters
  - Multiphase converters
- 10pin 3x3 DFN lead free package
- RoHS compliant

DESCRIPTION

The IR3720 measures the output voltage and inductor current of low-voltage DC-to-DC converters and reports the average power over a user specified time interval as a digital word on the I²C. The output current is measured across a current sensing resistor or indirectly across the inductor's DCR winding resistance. Additionally, the current measurement method is also applicable to multiphase converters.

The real time voltage and current signals are multiplied, digitized, and averaged over a user selectable averaging interval providing Patent Pending TruePower™ measurement of highly dynamic loads.

TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION

Device	Package	Order Quantity
IR3720MTRPBF	10 lead DFN (3x3 mm body)	3000 piece reel
* IR3720MPBF	10 lead DFN (3x3 mm body)	121 Piece tube

* Samples only

ABSOLUTE MAXIMUM RATINGS

All voltages referenced to GND
VDD: 3.9V
ALERT#:.....3.9V
ALERT#.....<VDD + 0.3V
EXTCLK 3.9V
All other Analog and Digital pins.....3.9V

Operating Junction Temperature....-10°C to 150°C
Storage Temperature Range.....-65°C to 150°C
Thermal Impedance (θ_{JC}).....53°C/W
ESD Rating .....HBM Class 2 JEDEC Standard
MSL Rating .....Level 2
Reflow Temperature .....260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply: VDD = 3.3V ± 5%, 0°C ≤ T_J ≤ 125°C, 0.5 ≤ VO ≤ 1.8 V, and operation in the system accuracy test circuit. See notes following table.

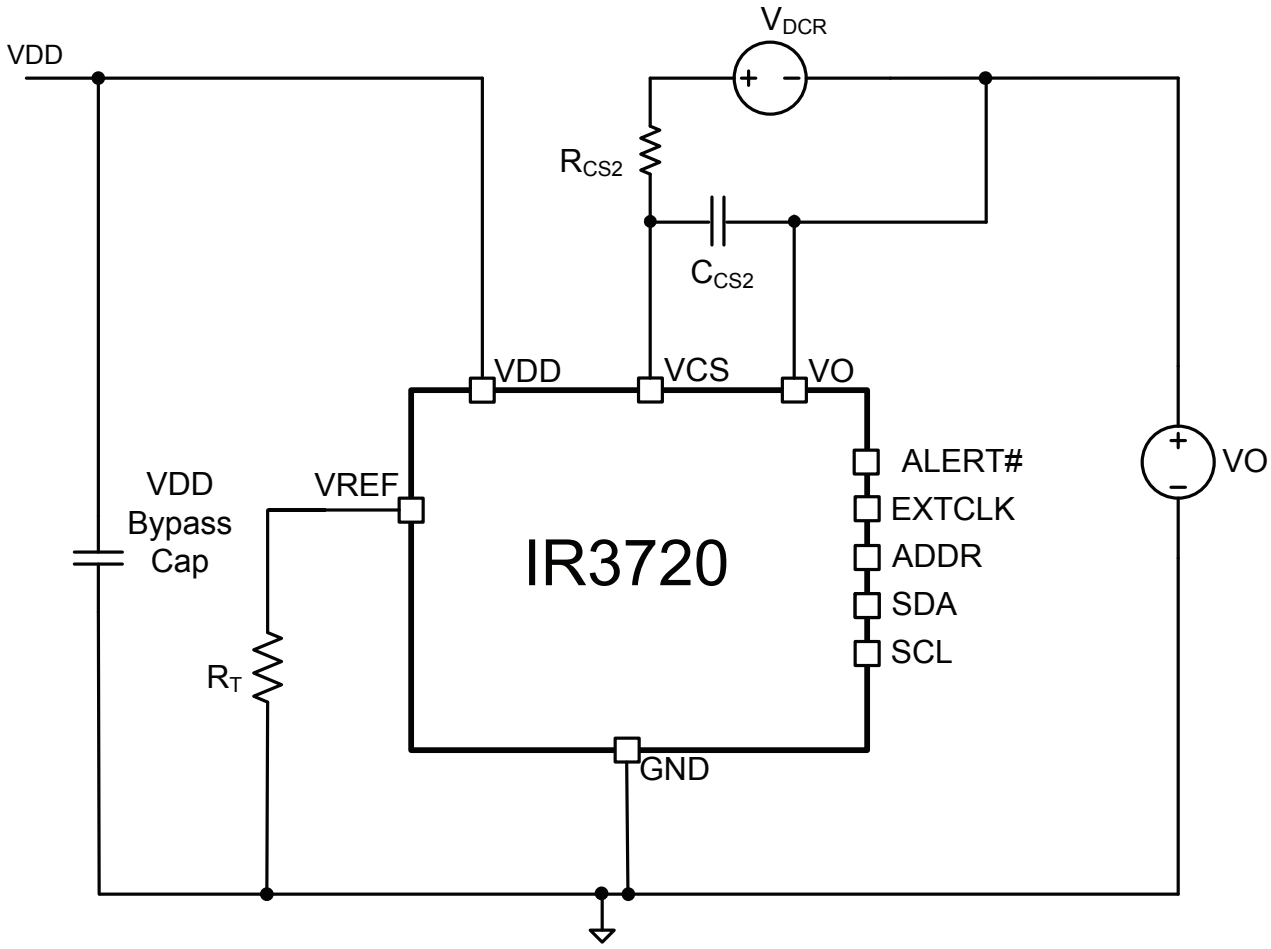
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
IC SYSTEM ACCURACY					
Power accuracy, IC only	R_{CS2} = 600 Ω, R_T = 25.5 kΩ, V_{DCR} = 20 mV, VO=1 volt, C_{CS2} = 1µF Sampling frequency 512 kHz. Sampling interval 8 ms, 0°C ≤ T_J ≤ 85°C Notes 1, 2			3.3	%
BIAS SUPPLY					
VDD Turn-on Threshold, VDD_{UP}				3.1	V
VDD Turn-off Threshold, VDD_{DN}		2.4			V
VDD Operating Current	R_T = 25.5 kΩ		480	660	µA
VDD Shutdown Current	Config Reg enable bit d4=1		17	100	µA
VOLTAGE REFERENCE					
V_{REF} Voltage	R_T = 25.5 kΩ	1.4	1.5	1.6	V
Reference load, R_T	Note 1	20	25.5	40	kΩ
VOLTAGE SENSOR					
Voltage error	VO=1V; V_{DCR}=0 mV, 0°C ≤ T_J ≤ 85°C R_{CS2}=600 Ω, R_T=25.5 kΩ, Note 1	-0.75		0.75	%
Voltage, full scale V_{FS}			1.854		V
CURRENT SENSOR					
Voltage, Current Gain, V_{IG}	R_T = 25.5 kΩ		1.5		V
Current range, Io x DCR	RCS2=600 Ω , R_T=25.5 kΩ	-35		35	mV
Current error	VO=1V; V_{DCR}=20 mV, 0°C ≤ T_J ≤ 85°C RCS2=600 Ω, R_T=25.5 KΩ, Note 1	-2.4		2.4	%

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
DIGITIZER					
Internal Sampling frequency	Driven from internal clock	435	512	589	kHz
External Sampling frequency	Driven from external clock	922	1024	1126	kHz
Transition time	Driven from external clock Note 1			50	ns
POWER INFORMATION					
Minimum Averaging Interval	Config Reg [d3..d0] = b‘0000, Note 1	0.9	1	1.1	ms
Maximum Averaging Interval	Config Reg [d3..d0] = b‘1000, Note 1	230	256	282	ms
Output Register Measuring power	VO=1V; V_{DCR}=20 mV R_{CS2}=600 Ω , R_T=25.5 kΩ, Note 1,2	1380	1440	1500	HEX
Output Register Measuring power	VO=0.5V; V_{DCR}=20 mV R_{CS2}=600 Ω, R_T=25.5 kΩ, Note 1,2	0980	0A00	0A80	HEX
Output Register Measuring power	VO=1V; V_{DCR}=0 mV R_{CS2}=600 Ω, R_T=25.5 kΩ, Note 1,2	FF40	0000	00C0	HEX
Output Register Measuring power	VO=1V; V_{DCR}=-8 mV R_{CS2}=600 Ω, R_T=25.5 kΩ, Note 1,2	F740	F800	F8C0	HEX
Full Scale Output Register Measuring power	VO = 1.8; V_{DCR}=35 mV R_{CS2}=600 Ω, R_T=25.5 kΩ, Note 1,2	3DC0	3F80	4000	HEX
DIGITAL INPUT AND OUTPUT					
ALERT# pull down resistance	Sink 3 mA			250	Ω
SDA & SCL HIGH Level	Note 1	2.1			V
SDA & SCL Low Level	Note 1			0.8	V
SCL Input current	Note 1	-5		+5	uA
SDA pull down voltage	Sink 4 mA Note 1			0.4	V
TIMING					
Maximum Frequency	Note 1	10		400	kHz
Bus free time between stop and start T_{BUF}	Note 1	1.3			us
Hold time after (repeated) start condition $T_{HD:STA}$	Note 1	0.6			us
Repeated start condition setup time $T_{SU:STA}$	Note 1	0.6			us
Stop condition setup time $T_{SU:STO}$	Note 1	0.6			us
Data hold time $T_{HD:DAT}$	Note 1	300			ns
Data setup time $T_{SU:DAT}$	Note 1	100			ns
Clock low period T_{LOW}	Note 1	1.3			us
Clock high period T_{HIGH}	Note 1	0.6			us
Clock or data fall time T_F	Note 1	20		300	ns
Clock or data rise time T_R	Note 1	20		300	ns

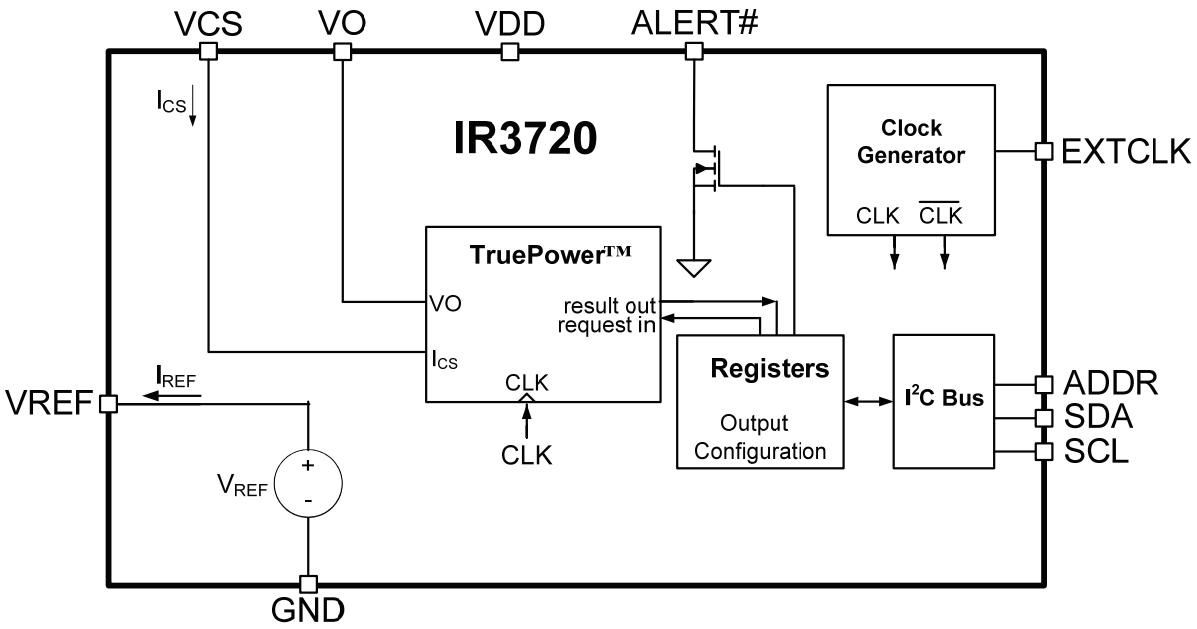
NOTE:

1. Guaranteed by design, not tested in production
2. Average of eight data samples

SYSTEM ACCURACY TEST CIRCUIT



BLOCK DIAGRAM



IC PIN DESCRIPTION

NAME	NUMBER	I/O LEVEL	DESCRIPTION
VCS	1	Analog	Current sensing input
VO	2	Analog	Voltage sensing input
VREF	3	Analog	Thermistor sensing input
GND	4		IC bias supply and signal ground
VDD	5	3.3V	3.3V bias supply
EXTCLK	6	3.3V Digital	Input for optional external clock
ADDR	7	3.3V Digital	I^2C Address selection input; See Table 1 for address
SCL	8	3.3V Digital	I^2C Clock; Input only
SDA	9	3.3V Digital	I^2C Data; Input / Open drain output
ALERT#	10	3.3V Digital	Programmable output function; Open drain output clamped to VDD
BASE PAD			Connect to pin 4

IC PIN FUNCTIONS

VDD PIN

This pin provides operational bias current to circuits internal to the IR3720. Bypass it with a high quality ceramic capacitor to the GND pin.

GND PIN

This pin returns operational bias current to its source. It is also the reference to which the voltage VO is measured, and it sinks the reference current established by the external resistor R_T.

VO PIN

Connect this pin to the location in the circuit where voltage for the power calculation is desired to be monitored. Since it also measures DCR voltage drop it is critical that it be Kelvin connected to the buck inductor output. Power accuracy may be degraded if the voltage at this pin is below VO_{min}.

VCS PIN

The average current into this pin is used to calculate power. A switched current source internal to the IR3720 will maintain the average voltage of this pin equal to the voltage of the VO pin.

VREF FUNCTION

A voltage reference internal to the IR3720 drives the V_{REF} pin while the pin current is monitored and used to set the amplitude of the current monitor switched current source I_{REF}. This pin should be connected to GND through a precision resistor network R_T. This network may include provision for canceling the positive temperature coefficient of the buck inductor's DC resistance (DCR).

ALERT# FUNCTION

The ALERT# pin is a multi-use pin. During normal use it can be configured via the I^2C as an open drain ALERT# pin that will be driven logic low when new data is available in the output register. After the output register has been read via the I^2C the ALERT# will be released to its high resistance state. This pin can also be programmed to pull low when the output exceeds the programmable level.

ADDR PIN

The ADDR pin is an input that establishes the I^2C address. Valid addresses are selected by grounding, floating, or wiring to VDD the ADDR pin. Table 1, "User Selectable Addresses", provides a mapping of possible selections.

Table 1 User selectable addresses

ADDR pin configuration	I^2C Address
Low	b'1110 000
Open	b'1110 010
High	b'1110 110

EXTCLK

This pin is a Schmitt trigger input for an optional externally provided square wave clock. The duty ratio of this externally provided clock, if used, shall be between 40% and 60%. If no external clock is used, connect this pin to GND and the internal clock will be used.

SCL

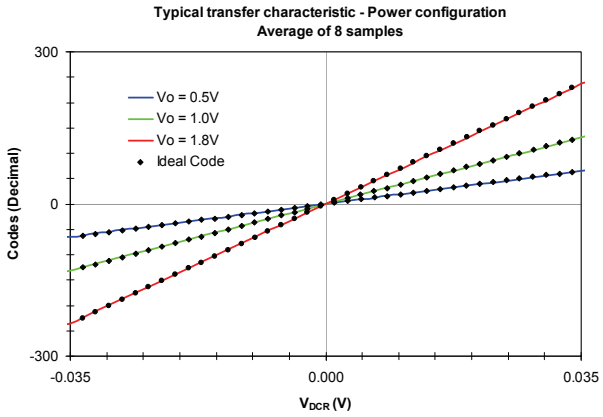
SCL is the I^2C clock and is capable of functioning with a rate as low as 10 kHz. It will continue to function as the rate is increased to 400 kHz. This device is considered a slave, and therefore uses the SCL as an input only.

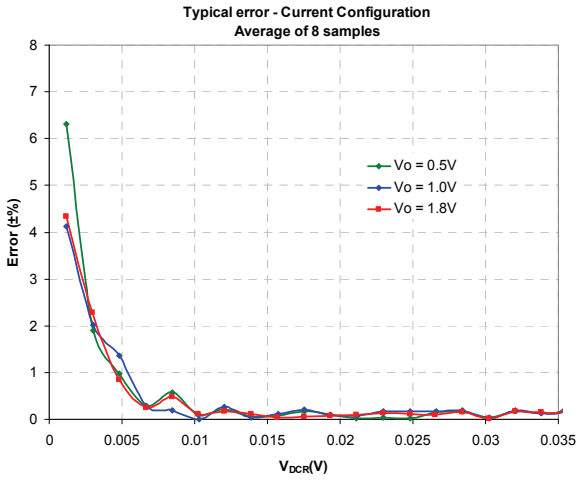
SDA

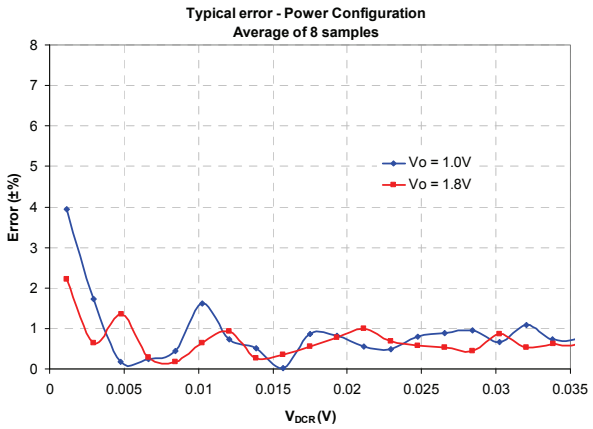
SDA is monitored as data input during master to slave transactions, and is driven as data output during slave to master transactions as indicated in the Packet Protocol section to follow.

TYPICAL PERFORMANCE CHARACTERISTICS

(System Accuracy Test Circuit, VDD=3.3 V, R_{CS2} = 600 Ω, C_{CS2} = 1 µF, R_T = 25.5 k Ω)







FUNCTIONAL DESCRIPTION

Please refer to the Functional Description Diagram below. Power flow from the buck converter is the product of output voltage times the current I_L flowing through the inductor.

Average power is measured with the aid of International Rectifier's proprietary TruePower™ circuit. Voltage, current, or the product of voltage Vo and current is digitized over the interval of interest and ported to the OUTPUT register. The VCS pin is maintained at an average voltage equal to Vo.

The full-scale voltage that can be measured is V_{FS}.

The full-scale positive current that can be measured is

$$I_{FS} = \frac{V_{IG}}{R_T} \cdot \frac{(R_{CS1} + R_{CS2})}{DCR} . \quad (1)$$

Full-scale current capability is designed by specifying the external circuit values of equation 1.
The full scale power P_{FS} that can be measured is the product of full-scale voltage and full scale current.

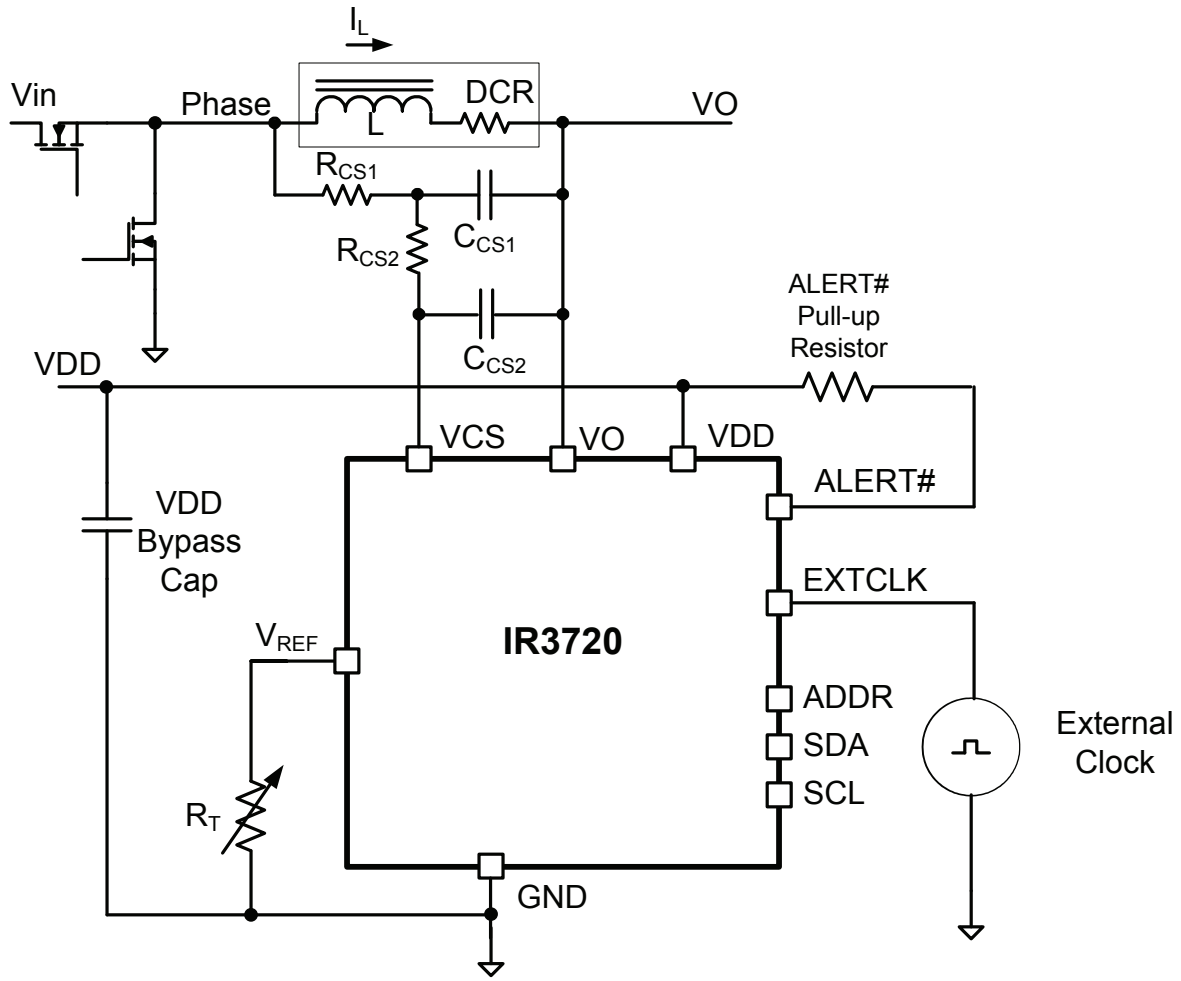


Figure 1 Functional Description Diagram

RESISTOR SENSING APPLICATION

The voltage on the shunt resistor of the circuit below is directly proportional to the current from the source. Shunts developing 5 mV to 75 mV at I_{FS} have been used. Accuracy is enhanced at the higher voltage. Select R_T to be a 25.5 kΩ 1% or better initial tolerance resistor. This value will sink 1.5V /R_T of current from the VREF pin of the IR3720.

R_{CS2} should be chosen such that this current through it develops the same voltage that is developed by the shunt at full scale current.
C_{CS2} is the integrator capacitor and should be between 0.1 µF and 10 µF.

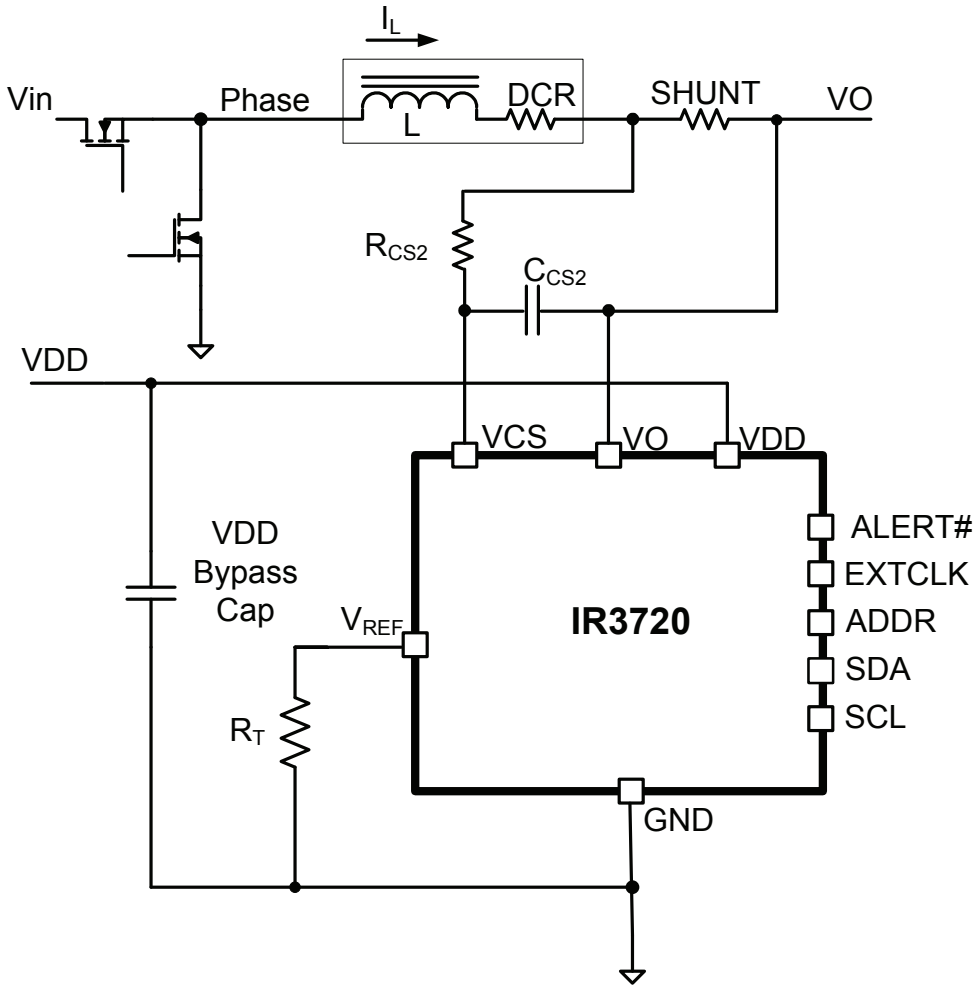


Figure 2 Resistor Sensing Circuit

INDUCTOR DCR CURRENT SENSING APPLICATION

Referring to the Functional Description Diagram, it can be seen that the shunt function can be accomplished by the DC resistance of the inductor that is already present. Omitting the resistive shunt reduces BOM cost and increases efficiency. In exchange for these two significant advantages two easily compensated design complications are introduced, a time constant and a temperature coefficient.

The inductor voltage sensed between the Rcs1 resistors is not simply proportional to the inductor current, but rather is expressed in the Laplace equation below.

$$V_L = I_L \cdot DCR\left(1 + s\frac{L}{DCR}\right)$$

This inductor time constant is canceled when

$$\frac{L}{DCR} = \frac{R_{CS1} \cdot R_{CS2}}{R_{CS1} + R_{CS2}} \cdot C_{CS1}.$$

Let $\frac{R_{CS1} \cdot R_{CS2}}{R_{CS1} + R_{CS2}} = R_{eq}$.

A second equation is used to set the full scale inductor current.

$I_{FS} = \frac{V_{IG}}{R_T} \cdot \frac{(R_{CS1} + R_{CS2})}{DCR}$. Let

$R_{CS1} + R_{CS2} = R_{sum}$ and solve for Rsum.

Select a standard value C_{CS1} that is larger than $\frac{4 \cdot L}{DCR \cdot R_{SUM}}$. Solve for R_{eq}.

We now know Req and Rsum, but we do not know the individual resistor values R_{CS1} or R_{CS2}. The next step is to solve for them simultaneously. By substituting R_{sum} into the R_{eq} equation the following can be written:

$R_{eq} = \frac{R_{CS1} \cdot R_{CS2}}{R_{sum}}$, which can then be rearranged to

$$R_{CS1}^2 - R_{CS1} \cdot R_{sum} + R_{eq} \cdot R_{sum} = 0 .$$

Note that this equation is of the form $ax^2 + bx + c = 0$ where a=0, b=-Rsum, and c=Req•Rsum. The roots of this quadratic equation will be R_{CS1} and R_{CS2}. Use the higher value resistor as R_{CS1} in order to minimize ripple current in C_{CS1}.

$$R_{CS1} = R_{SUM} \cdot \frac{1 + \sqrt{1 - 4 \cdot \frac{R_{eq}}{R_{SUM}}}}{2}$$

and

$$R_{CS1} = R_{SUM} \cdot \frac{1 - \sqrt{1 - 4 \cdot \frac{R_{eq}}{R_{SUM}}}}{2}$$

THERMAL COMPENSATION FOR INDUCTOR DCR CURRENT SENSING

The positive temperature coefficient of the DCR can be compensated if R_T varies inversely proportional to the DCR. DCR of a copper coil, as a function of temperature, is approximated by

$$DCR(T) = DCR(T_R) \cdot (1 + (T - T_R) \cdot TCR_{Cu}) \quad . \qquad (2)$$

T_R is some reference temperature, usually 25 °C, and TCR_{Cu} is the resistive temperature coefficient of copper, usually assumed to be 0.0039 near room temperature. Note that equation 2 is linearly increasing with temperature and has an offset of $DCR(T_R)$ at the reference temperature.
If R_T incorporates a negative temperature coefficient thermistor then temperature effects of DCR can be minimized. Consider a circuit of two resistors and a thermistor as shown below.

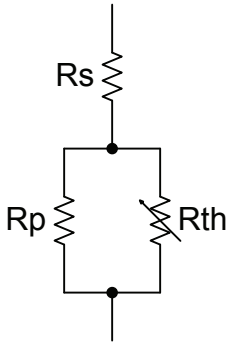


Figure 3 R_T Network

If Rth is an NTC thermistor then the value of the network will decrease as temperature increases. Unfortunately, most thermistors exhibit far more variation with temperature than copper wire. One equation used to model thermistors is

$$R_{th}(T) = R_{th}(T_0) \cdot e^{\left(\beta\left(\frac{1}{T} - \frac{1}{T_0}\right)\right)} \qquad (3)$$

where $R_{th}(T)$ is the thermistor resistance at some temperature T, $R_{th}(T_0)$ is the thermistor resistance at the reference temperature T_0, and β is the material constant provided by the thermistor manufacturer. Degrees Kelvin are used in equation 3. If R_S is large and R_P is small, the curvature of the effective network resistance can be reduced from the curvature of the thermistor alone. Although the exponential equation 3 can never compensate linear equation 2 at all temperatures, a spreadsheet can be constructed to minimize error over the temperature interval of interest. The resistance R_T of the network shown as a function of temperature is

$$R_T(T) = R_s + \frac{1}{\frac{1}{R_p} + \frac{1}{R_{th}(T)}} \qquad (4)$$

using $R_{th}(T)$ from equation 3.
Equation 1 of the last section may be rewritten as a new function of temperature using equations 2 and 4 as follows:

$$I_{FS}(T) = \frac{V_{IG}}{R_T(T)} \cdot \frac{(R_{CS1} + R_{CS2})}{DCR(T)} . \qquad (5)$$

With Rs and Rp as additional free variables, use a spreadsheet to solve equation 5 for the desired full scale current while minimizing the $I_{FS}(T)$ variation over temperature.

TYPICAL 2-PHASE DCR-SENSING APPLICATION

The IR3720 is capable of monitoring power in a multiphase converter. A two-phase circuit is shown below. The voltage output of any phase is equal to that of any and every other phase, and monitored at VO as before.

Output current is the sum of the two inductor currents (I_{L1} + I_{L2}). Superposition is used to derive the transfer function for multiphase sensing. The voltage on R_{CS2} due to I_{L1} is

$$I_{L1} \cdot DCR_1 \cdot \frac{(R_{CS2} \parallel R_{CS3})}{R_{CS1} + (R_{CS2} \parallel R_{CS3})}$$

Likewise, the voltage on R_{CS2} due to I_{L2} is

$$I_{L2} \cdot DCR_2 \cdot \frac{(R_{CS2} \parallel R_{CS1})}{R_{CS3} + (R_{CS2} \parallel R_{CS1})}$$

The current through R_{CS2} due to both inductor currents is I_{CS}. From the two equations above

$$I_{CS} = \frac{I_{L1} DCR_1 R_{CS3} + I_{L2} DCR_2 R_{CS1}}{R_{CS1}R_{CS2} + R_{CS1}R_{CS3} + R_{CS2}R_{CS3}}$$

If DCR_1=DCR_2, and R_{CS1}=R_{CS3}, then I_{CS} can be simplified to

$$I_{CS} = \frac{(I_{L1} + I_{L2}) \cdot DCR_1}{R_{CS1} + 2R_{CS2}}$$

Full scale I_{CS} current corresponds to

$$I_{CSFS} = \frac{V_{IG}}{R_T}$$

which yields 256 digital current counts (0100 0000 0000 0000).

Full scale total inductor current is

$$(I_{L1} + I_{L2})_{FS} = \frac{V_{IG}}{R_T} \cdot \frac{(R_{CS1} + 2 \cdot R_{CS2})}{DCR}$$

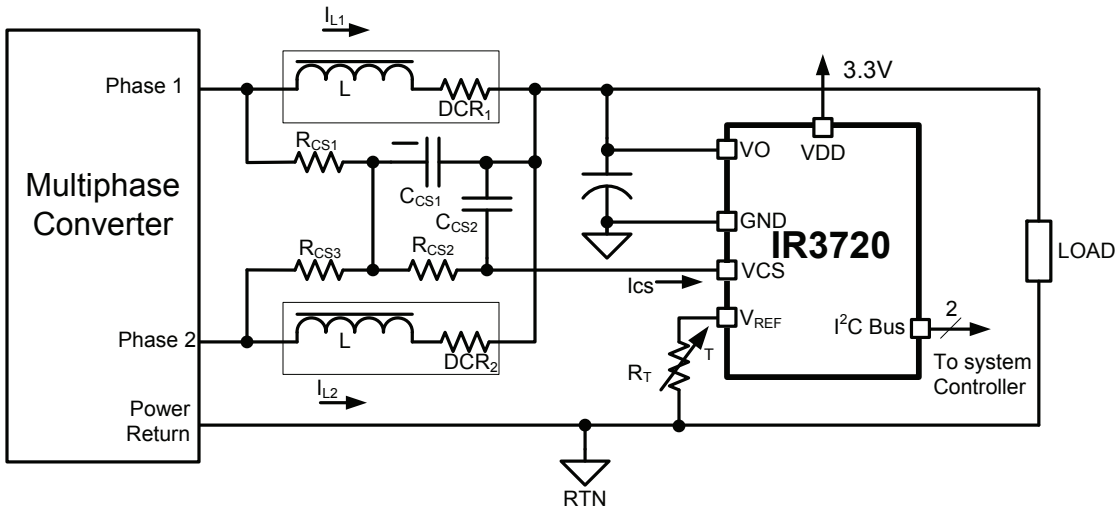


Figure 4Two Phase DCR Sensing Circuit

ERROR MANAGEMENT

Component value errors external to the IR3720 contribute to power and current measurement error. The power reported by the IR3720 is a function not only of actual power or current, but also of products and quotients of R_T, R_{CS1}, R_{CS2}, DCR (or R_{SHUNT}), as well as parameters internal to the IR3720. The tolerance of these components increases the total power or current error. Small signal resistors are typically available in 1% tolerance, but 0.1% parts are available. Shunts are also available at 1% or 0.1% tolerance. The DCR tolerance of inductors can be 5%, but 3% are available. Fortunately, it is not typical that worst-case errors would systematically stack in one direction. It is statistically likely that a high going value would be paired with a low going value to somewhat cancel the error. Because of this, tolerances can be added in quadrature (RSS). As an example, a 3% DCR used with a 1% R_T, a 1% R_{CS}, and 3.3% IR3720 contributes

$$\sqrt{(0.03)^2+(0.01)^2+(0.01)^2+(0.033)^2} \approx 4.7\%$$

error to a typical system.

Quantization error occurs in digital systems because the full scale is partitioned into a finite number of intervals and the number of the interval containing the measured value is reported. It is not likely that the measured value would correspond exactly to the center of the interval. The error could be as large as half the width of the interval. With a binary word size of eight, full scale is partitioned into 255 intervals. Consider a measurement made near full scale. Any signal in this interval is less than ± .2% (one-half of 100% / 256) away from the interval's center, and would therefore never have more error than that due to quantization. On the other hand, consider a measurement at one-tenth full scale. One-half of an interval size at this level corresponds to 2% of the reported value! Relative quantization error increases as the measured value becomes small compared to the full-scale value.
Quantization error can be reduced by averaging a sequence of returned values.

CONFIGURATION REGISTER

A configuration register is maintained via the I^2C MFR_SPECIFIC_00 command, code # D0h. The low order nibble (d3, d2, d1, d0) contains a binary number N from zero to eight. The averaging interval is 2^N milliseconds. N defaults to zero on start up.

The next bit (d4) is to be used as a function enable bit. b'1 commands an energy saving shut down mode, and power on default b'0 commands fully functioning mode.

d5 high enables the EXTCLK pin to receive the external clock signal, and default d5 low enables the internal clock.

The next two bits (d7, d6) program the output parameter. B'00 causes power to be measured and is the power on default state. B'01 causes voltage to be measured. B'10 causes current to be measured. B'11 is not defined and should not be used.

The next bit (d8) is used to configure the ALERT# pin. b'0 is the power on default, and commands ALERT# being pulled low when new data is available. b'1 programs the ALERT# to pull low when the programmable threshold level is exceeded, whether it is power, voltage, or current.

Register bits (d15...d9) are the ALERT# threshold register. If the output register is larger than this register, and if (d8) is b'1, then the ALERT# pin will pull low. The two least significant bits of the output register are not represented in the ALERT# threshold register. d15…d9 defaults to zero on start up.

The results of a configuration register change will be reflected in the OUTPUT REGISTER after previously requested operations have completed.

BIT #	CONFIGURATION REGISTER
d0	Averaging interval (LSB)
d1	Averaging interval
d2	Averaging interval
d3	Averaging interval (MSB)
d4	Enable
d5	External clock
d6	OUTPUT config (LSB)
d7	OUTPUT config (MSB)
d8	ALERT# configuration
d9	ALERT# threshold (LSB + 2)
d10	ALERT# threshold
d11	ALERT# threshold
d12	ALERT# threshold
d13	ALERT# threshold
d14	ALERT# threshold
d15	ALERT# threshold (MSB)

OUTPUT REGISTER

The output register is loaded with a two's compliment factor of voltage, current, or power, depending on the last request loaded into the configuration register. I^2C "Direct Data Format" is used. The value of the output register is to be multiplied by a scale factor that is derived from equations 1 and 2 above. Maximum power is the product of maximum voltage and maximum current.
The range of valid values is indicated in Table 2 below.

Table 2 Output Register Range of Returned Values

Parameter	Returned value (twos compliment binary)	Returned value (decimal)
FS voltage	0100 0000 0000 0000	256
Zero voltage	0000 0000 0000 0000	0
+FS current	0100 0000 0000 0000	256
-FS current	1100 0000 0000 0000	-256
+FS power	0100 0000 0000 0000	256
-FS power	1100 0000 0000 0000	-256

A binary point is implicitly located to the left of the first six least significant figures, as in the example below.

SYYY YYYY YY.00 0000

The "S" above is the twos compliment sign bit, and the "Y's" are the twos compliment. Six zeros pad out the two byte response. These padding zeros could be considered a factor of the slope, which is allowed by the Direct Data Format. The output register multiplied by its scale factor K_x yields the requested quantity in engineering units of volts, amps, or watts.

The equations below convert digital counts to engineering units:

$$\text{Voltage} = \text{counts} \cdot \frac{V_{FS}}{256}$$ when configuration register bits (d7, d6) are set to (01).

$$\text{Current} = \text{counts} \cdot \frac{V_{IG} \cdot (R_{CS1} + R_{CS2})}{256 \cdot R_T \cdot DCR}$$ when configuration register bits (d7, d6) are set to (10).

$$\text{Power} = \text{counts} \cdot \frac{V_{FS} \cdot V_{IG} \cdot (R_{CS1} + R_{CS2})}{256 \cdot R_T \cdot DCR}$$ when configuration register bits (d7, d6) are set to (00).

There is but one output register, and it holds the measurement type (voltage, current, or power) last requested by the configuration register. It is incumbent upon the user to establish correct configuration before requesting a read. READ_VOUT, READ_IOUT, and READ_POUT are equivalent in that each returns the contents of the same output register.

BIT#	OUTPUT REGISTER
d15:d0	Output variable, D0 is LSB

RESERVED COMMAND CODES

Command codes D2h through D5h, D7h, and D8h are reserved for manufacturing use only and could lead to undesirable device behavior.

PACKET PROTOCOL

S = Start Condition
W = Bus write (lo)
R = Bus read (hi)
A = Acknowledge, = 0 for ACK, =1 for NACK
P = Stop Condition

	=	master to slave
	=	slave to master

Bus Write CONFIGURATION Register

S	Slave Address	W	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P
S	see Table 1	0	A	1 1 0 1 0 0 0 0	A	d7 d6 d5 d4 d3 d2 d1 d0	A	d15 d14 d13 d12 d11 d10 d9 d8	A	P

Bus Read CONFIGURATION Register

S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte Low	A	Data Byte High	A	P
S	see Table 1	0	A	1 1 0 1 0 0 0 0	A	S	See Table 1	1	A	d7 d6 d5 d4 d3 d2 d1 d0	A	d15 d14 d13 d12 d11 d10 d9 d8	1	P

Bus Read_VOUT (Output Register for Configuration register Data Byte Low = 01XXXXXX)

S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte Low	A	Data Byte High	A	P
S	see Table 1	0	A	1 0 0 0 1 0 1 1	A	S	See Table 1	1	A	d7 d6 d5 d4 d3 d2 d1 d0	A	d15 d14 d13 d12 d11 d10 d9 d8	1	P

Bus Read_IOUT (Output Register for Configuration register Data Byte Low = 10XXXXXX)

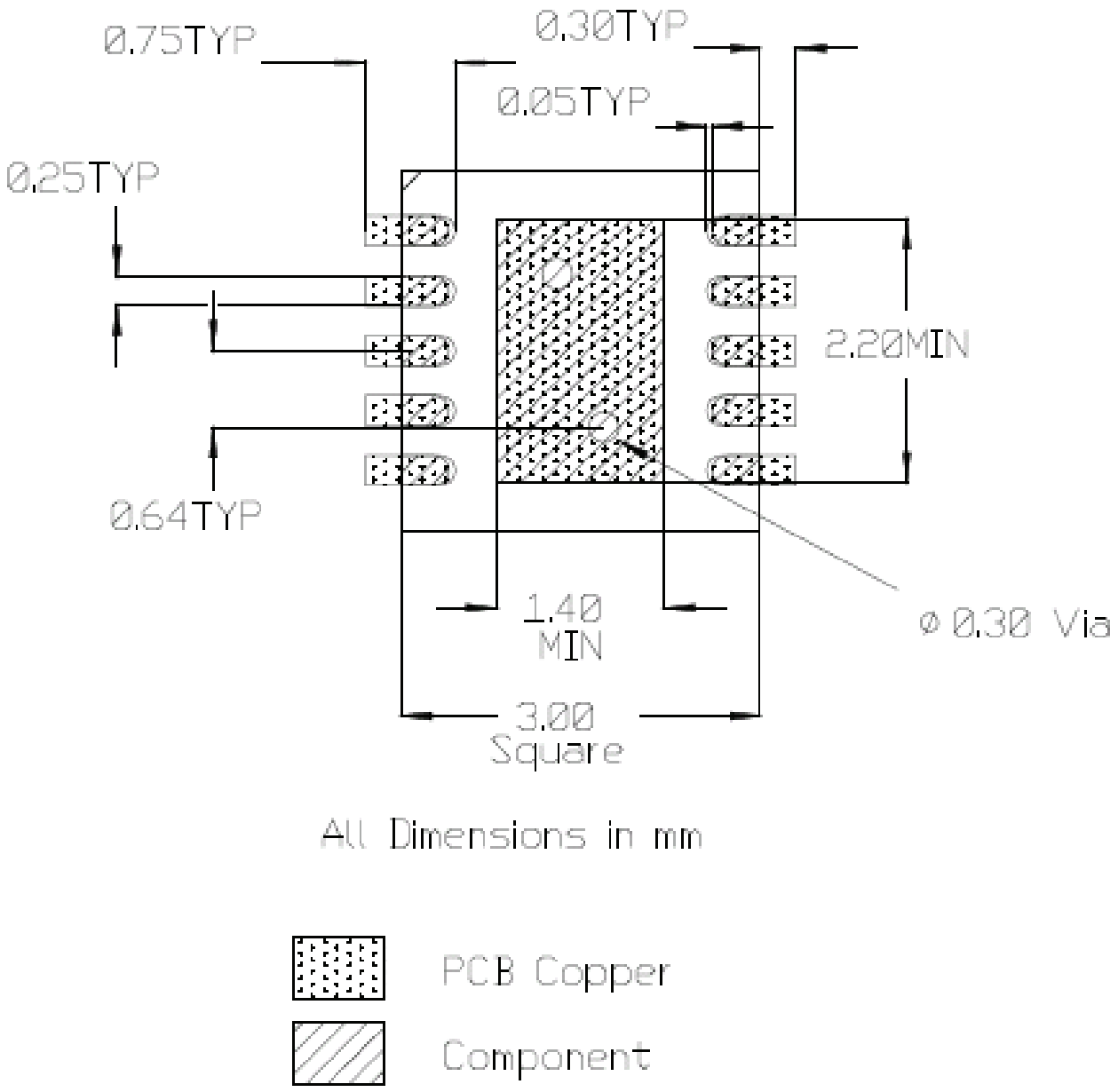
S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte Low	A	Data Byte High	A	P
S	see Table 1	0	A	1 0 0 0 1 1 0 0	A	S	See Table 1	1	A	d7 d6 d5 d4 d3 d2 d1 d0	A	d15 d14 d13 d12 d11 d10 d9 d8	1	P

Bus Read_POUT (Output Register for Configuration register Data Byte Low = 00XXXXXX)

S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte Low	A	Data Byte High	A	P
S	see Table 1	0	A	1 0 0 1 0 1 1 0	A	S	See Table 1	1	A	d7 d6 d5 d4 d3 d2 d1 d0	A	d15 d14 d13 d12 d11 d10 d9 d8	1	P

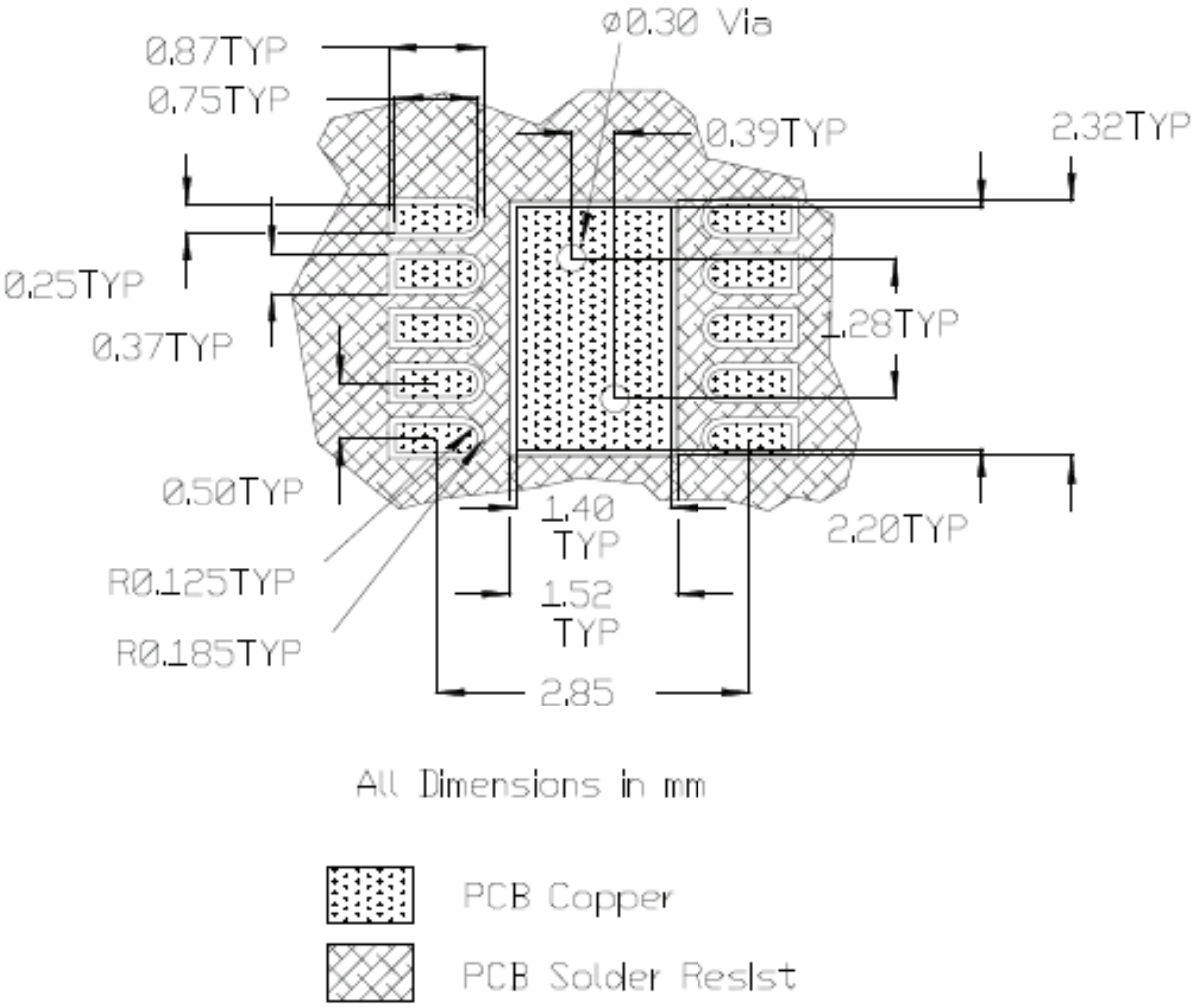
PCB PAD AND COMPONENT PLACEMENT

The figure below shows suggested pad and component placement.



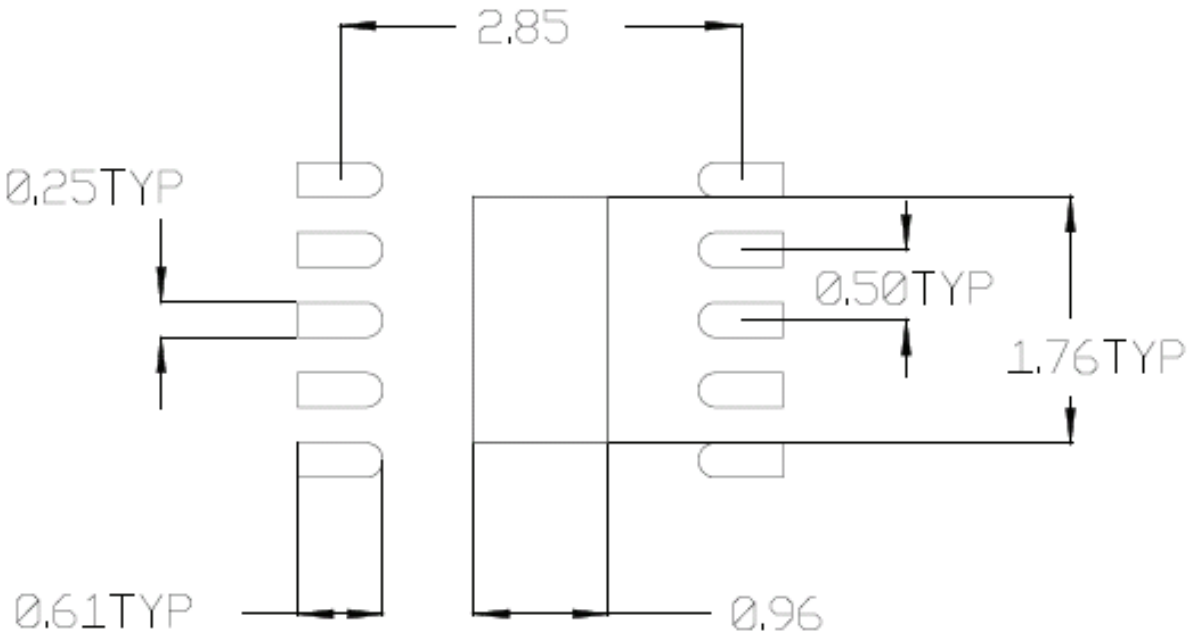
SOLDER RESIST

The figure below shows the suggested solder resist placement.



STENCIL DESIGN

The figure below shows a suggested stencil design.

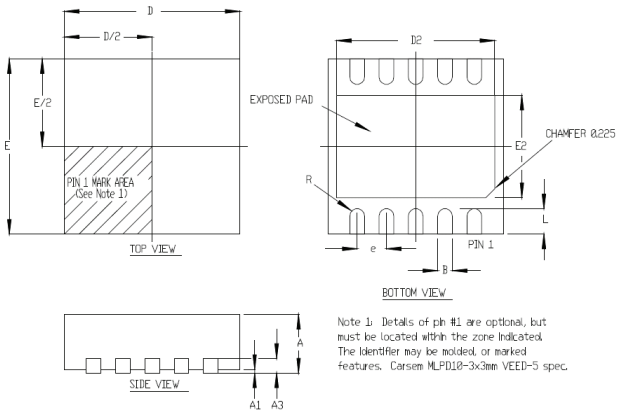


Stencil Aperture

All Dimensions in mm

PACKAGE INFORMATION

3X3 MM 10L DFN LEAD FREE



SYMBOL	10 PIN 3X3 MM		
DESIGN	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.18	0.23	0.30
D		3.00 BSC	
D2	2.20	---	2.70
E		3.00 BSC	
E2	1.40	---	1.75
e		0.50 BSC	
L	0.30	0.40	0.50
R	0.09	---	---

Data and specifications subject to change without notice.
This product has been designed and qualified for the consumer market.
Qualification standards can be found on IR's Web site.

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